

## Product Summary

$BV_{DSS}$	$R_{DS(ON)}$ Max	$I_D$ $T_C = +25^\circ C$
100V	9.5m $\Omega$ @ $V_{GS} = 10V$	29.5A

## Description and Applications

This new generation N-Channel Enhancement Mode MOSFET is designed to minimize  $R_{DS(ON)}$  and yet maintain superior switching performance. This device is ideal for use in Notebook battery power management and Loadswitch.

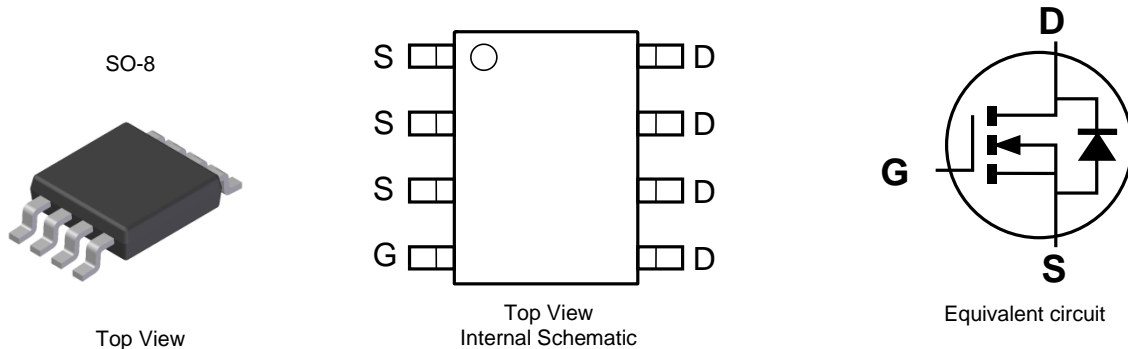
- Backlighting
- Power Management Functions
- DC-DC Converters

## Features and Benefits

- 100% Unclamped Inductive Switch (UIS) Test in Production
- High Conversion Efficiency
- Low  $R_{DS(ON)}$  – Minimizes On State Losses
- Low Input Capacitance
- Fast Switching Speed
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **Qualified to AEC-Q101 Standards for High Reliability**

## Mechanical Data

- Case: SO-8
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Connections Indicator: See Diagram
- Terminals: Finish — Matte Tin Annealed over Copper Leadframe. Solderable per MIL-STD-202, Method 208  $\text{E3}$
- Weight: 0.074 grams (Approximate)

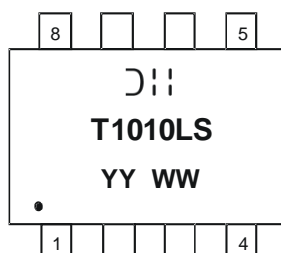


## Ordering Information (Note 4)

Part Number	Case	Packaging
DMT10H010LSS-13	SO-8	2,500/Tape & Reel

- Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
  2. See [http://www.diodes.com/quality/lead\\_free.html](http://www.diodes.com/quality/lead_free.html) for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
  3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
  4. For packaging details, go to our website at <http://www.diodes.com/products/packages.html>.

## Marking Information



- Diodes Incorporated symbol = Manufacturer's Marking
- T1010LS = Product Type Marking Code
- YYWW = Date Code Marking
- YY or YY = Year (ex: 15 = 2015)
- WW = Week (01 to 53)

**Maximum Ratings** (@T<sub>A</sub> = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Unit	
Drain-Source Voltage	V <sub>DSS</sub>	100	V	
Gate-Source Voltage	V <sub>GSS</sub>	±20	V	
Continuous Drain Current (Note 6), V <sub>GS</sub> = 10V	Steady State	T <sub>A</sub> = +25°C T <sub>A</sub> = +70°C	11.5 9.2	A
	Steady State	T <sub>C</sub> = +25°C T <sub>C</sub> = +100°C	29.5 18.6	A
Pulsed Drain Current (10µs Pulse, Duty Cycle = 1%)	I <sub>DM</sub>	75	A	
Maximum Continuous Body Diode Forward Current (Note 6)	I <sub>S</sub>	3	A	
Avalanche Current (Note 8), L=0.3mH	I <sub>AS</sub>	10	A	
Avalanche Energy (Note 8), L=0.3mH	E <sub>AS</sub>	15	mJ	

**Thermal Characteristics** (@T<sub>A</sub> = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Unit	
Total Power (Note 5)	P <sub>D</sub>	1.4	W	
Thermal Resistance, Junction to Ambient (Note 5)	Steady State t<10s	R <sub>θJA</sub>	90	°C/W
		R <sub>θJA</sub>	48.8	
Total Power Dissipation (Note 6)	P <sub>D</sub>	1.9	W	
Thermal Resistance, Junction to Ambient (Note 6)	Steady State t<10s	R <sub>θJA</sub>	66	°C/W
		R <sub>θJA</sub>	35.8	
Thermal Resistance, Junction to Case (Note 6)	R <sub>θJC</sub>	10.1	°C/W	
Operating and Storage Temperature Range	T <sub>J</sub> , T <sub>STG</sub>	-55 to +150	°C	

**Electrical Characteristics** (T<sub>A</sub> = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
<b>OFF CHARACTERISTICS (Note 7)</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	100	—	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = 1mA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	—	—	1	µA	V <sub>DS</sub> = 80V, V <sub>GS</sub> = 0V
Gate-Source Leakage	I <sub>GSS</sub>	—	—	±100	nA	V <sub>GS</sub> = ±20V, V <sub>DS</sub> = 0V
<b>ON CHARACTERISTICS (Note 7)</b>						
Gate Threshold Voltage	V <sub>GS(TH)</sub>	1.4	1.9	2.8	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250µA
Static Drain-Source On-Resistance	R <sub>DS(ON)</sub>	—	8	9.5	mΩ	V <sub>GS</sub> = 10V, I <sub>D</sub> = 13A
		—	9	12		V <sub>GS</sub> = 6V, I <sub>D</sub> = 13A
		—	10	14.5		V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 5A
Diode Forward Voltage	V <sub>SD</sub>	—	0.8	1.3	V	V <sub>GS</sub> = 0V, I <sub>S</sub> = 13A
<b>DYNAMIC CHARACTERISTICS (Note 8)</b>						
Input Capacitance	C <sub>ISS</sub>	—	2592	—	pF	V <sub>DS</sub> = 50V, V <sub>GS</sub> = 0V f = 1MHz
Output Capacitance	C <sub>OSS</sub>	—	792	—		
Reverse Transfer Capacitance	C <sub>RSS</sub>	—	45	—		
Gate Resistance	R <sub>g</sub>	—	2	—	Ω	V <sub>DS</sub> = 0V, V <sub>GS</sub> = 0V, f = 1MHz
Total Gate Charge	Q <sub>g</sub>	—	53.7	—	nC	V <sub>DD</sub> = 50V, I <sub>D</sub> = 13A, V <sub>GS</sub> = 10V
Gate-Source Charge	Q <sub>gs</sub>	—	10.6	—		
Gate-Drain Charge	Q <sub>gd</sub>	—	8.2	—		
Turn-On Delay Time	t <sub>D(ON)</sub>	—	11.6	—	ns	V <sub>DD</sub> = 50V, V <sub>GS</sub> = 10V, I <sub>D</sub> = 13A, R <sub>g</sub> = 6Ω
Turn-On Rise Time	t <sub>r</sub>	—	14.1	—		
Turn-Off Delay Time	t <sub>D(OFF)</sub>	—	42.9	—		
Turn-Off Fall Time	t <sub>f</sub>	—	22	—		
Reverse Recovery Time	t <sub>RR</sub>	—	49.8	—		
Reverse Recovery Charge	Q <sub>RR</sub>	—	85.1	—	nC	I <sub>F</sub> = 13A, di/dt = 100A/µs

- Notes:
5. Device mounted on FR-4 PC board, with minimum recommended pad layout, single sided.
  6. Device mounted on FR-4 substrate PC board, 2oz copper, with thermal bias to bottom layer 1inch square copper plate
  7. Short duration pulse test used to minimize self-heating effect.
  8. Guaranteed by design. Not subject to product testing.

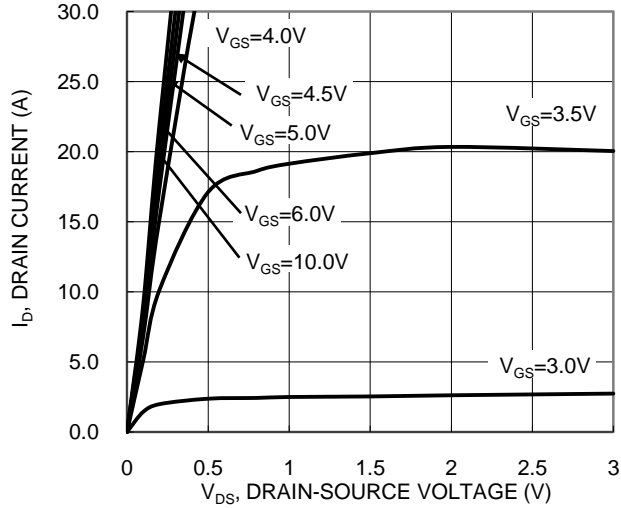


Figure 1. Typical Output Characteristic

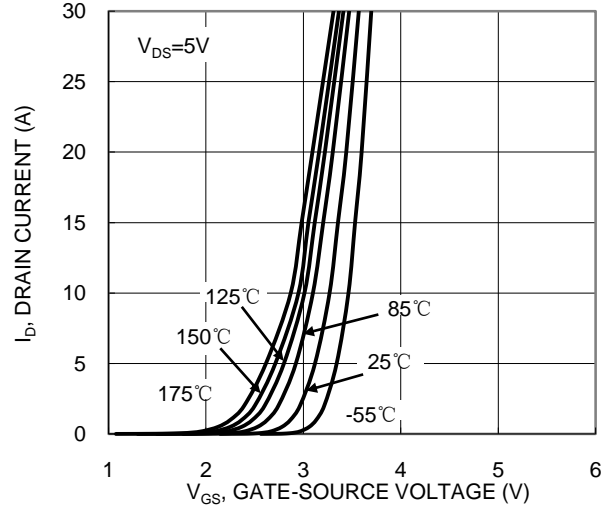


Figure 2. Typical Transfer Characteristic

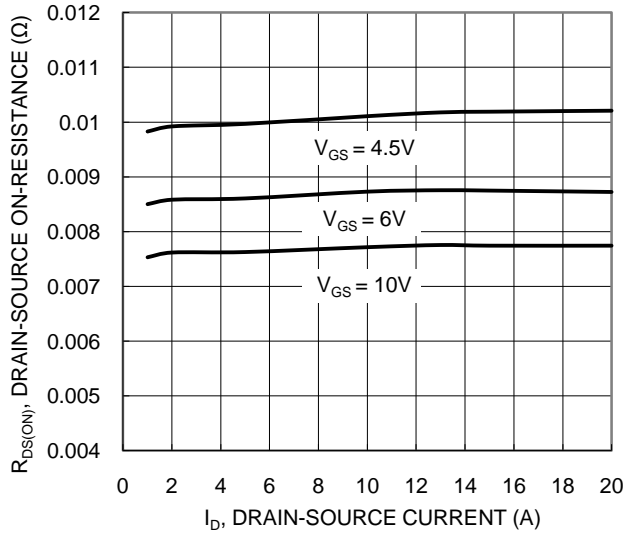


Figure 3. Typical On-Resistance vs. Drain Current and Gate Voltage

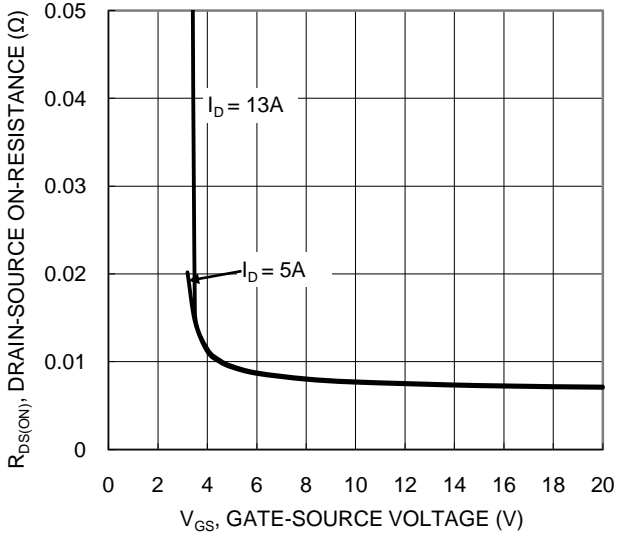


Figure 4. Typical Transfer Characteristic

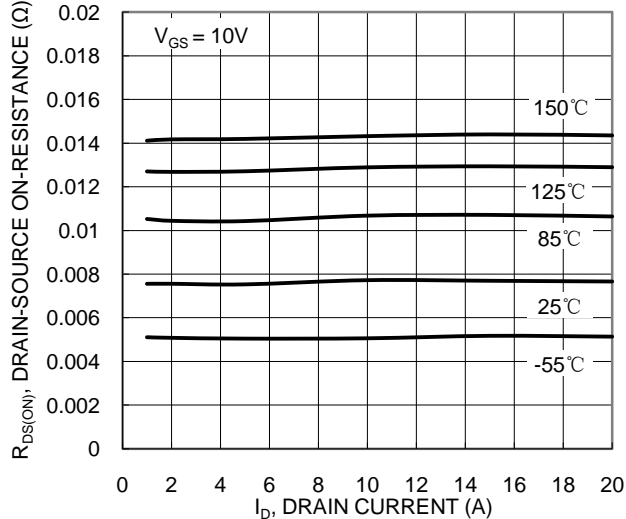


Figure 5. Typical On-Resistance vs. Drain Current and Temperature

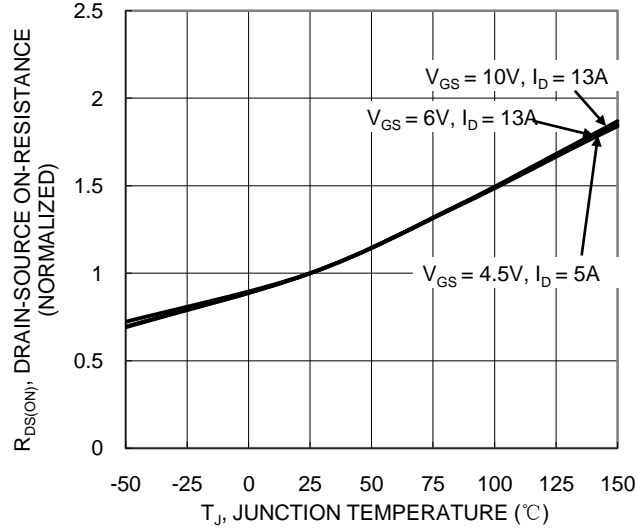


Figure 6. On-Resistance Variation with Temperature

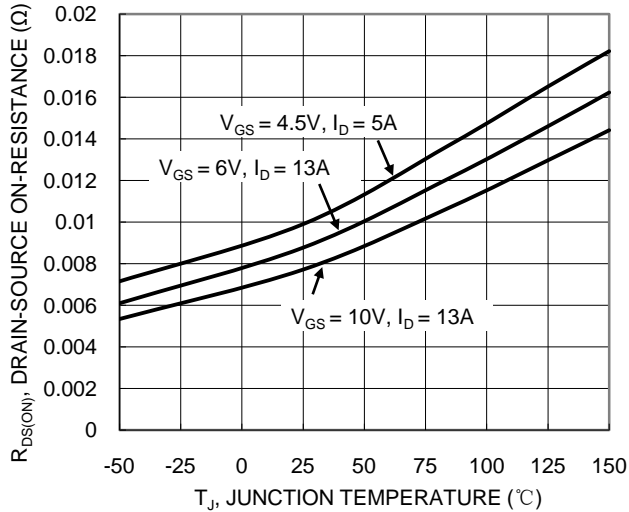


Figure 7. On-Resistance Variation with Temperature

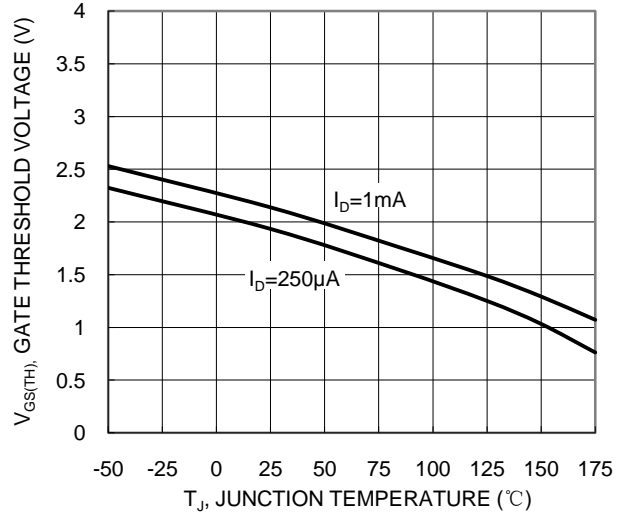


Figure 8. Gate Threshold Variation vs. Junction Temperature

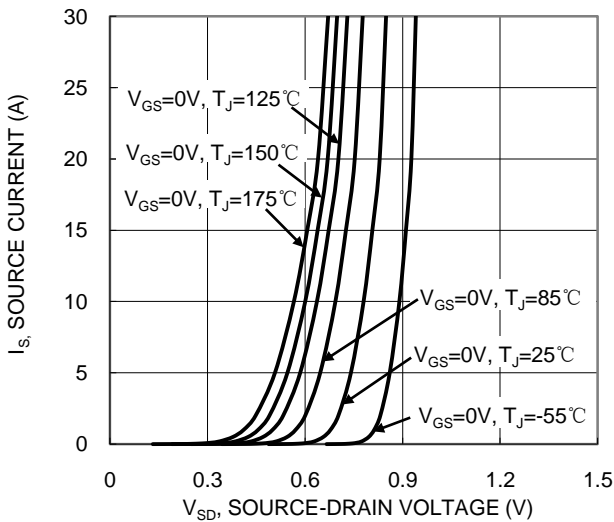


Figure 9. Diode Forward Voltage vs Current

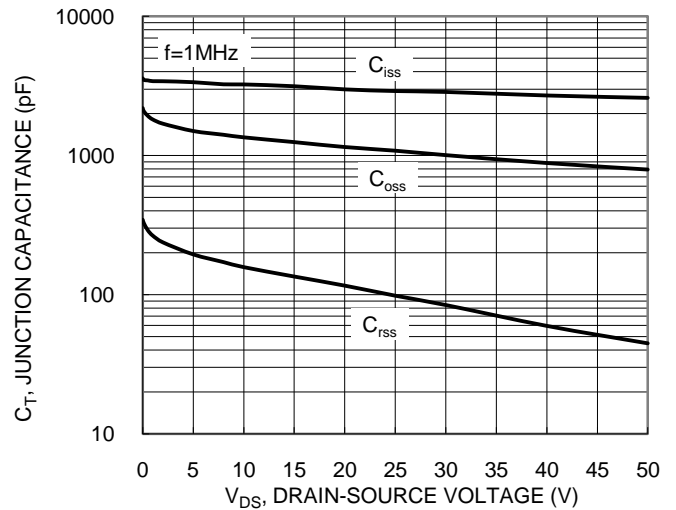


Figure 10. Typical Junction Capacitance

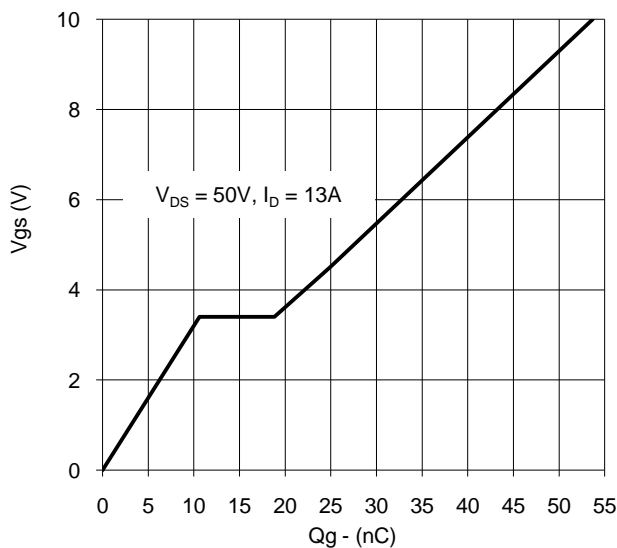


Figure 11. Gate Charge

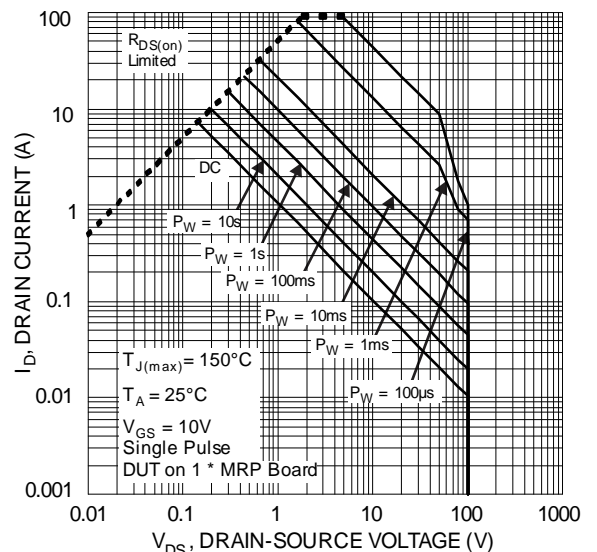
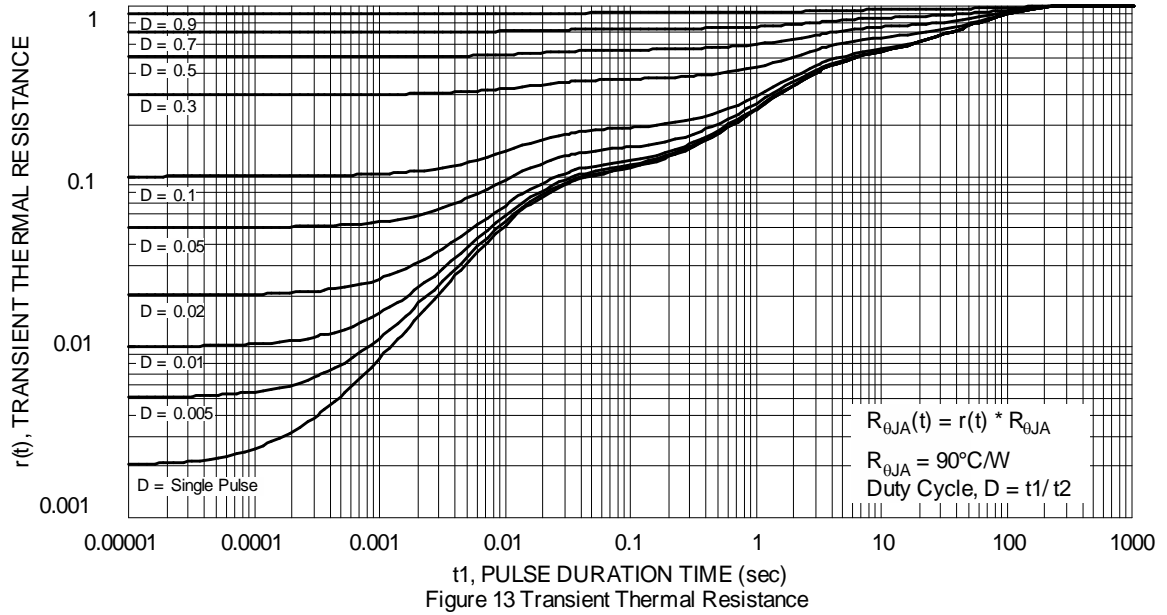


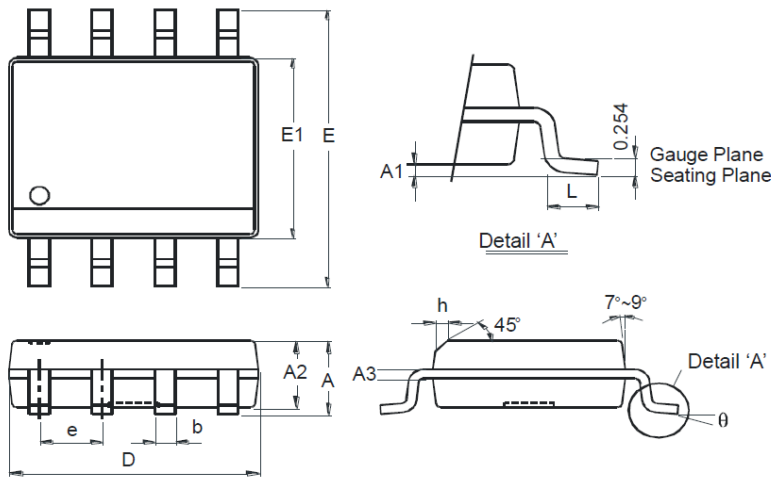
Figure 12 SOA, Safe Operation Area



**Package Outline Dimensions**

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

**SO-8**

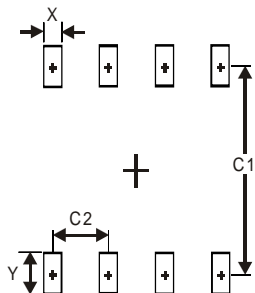


SO-8		
Dim	Min	Max
A	-	1.75
A1	0.10	0.20
A2	1.30	1.50
A3	0.15	0.25
b	0.3	0.5
D	4.85	4.95
E	5.90	6.10
E1	3.85	3.95
e	1.27 Typ	
h	-	0.35
L	0.62	0.82
θ	0°	8°
All Dimensions in mm		

**Suggested Pad Layout**

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

**SO-8**



Dimensions	Value (in mm)
X	0.60
Y	1.55
C1	5.4
C2	1.27

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